

FIG.1

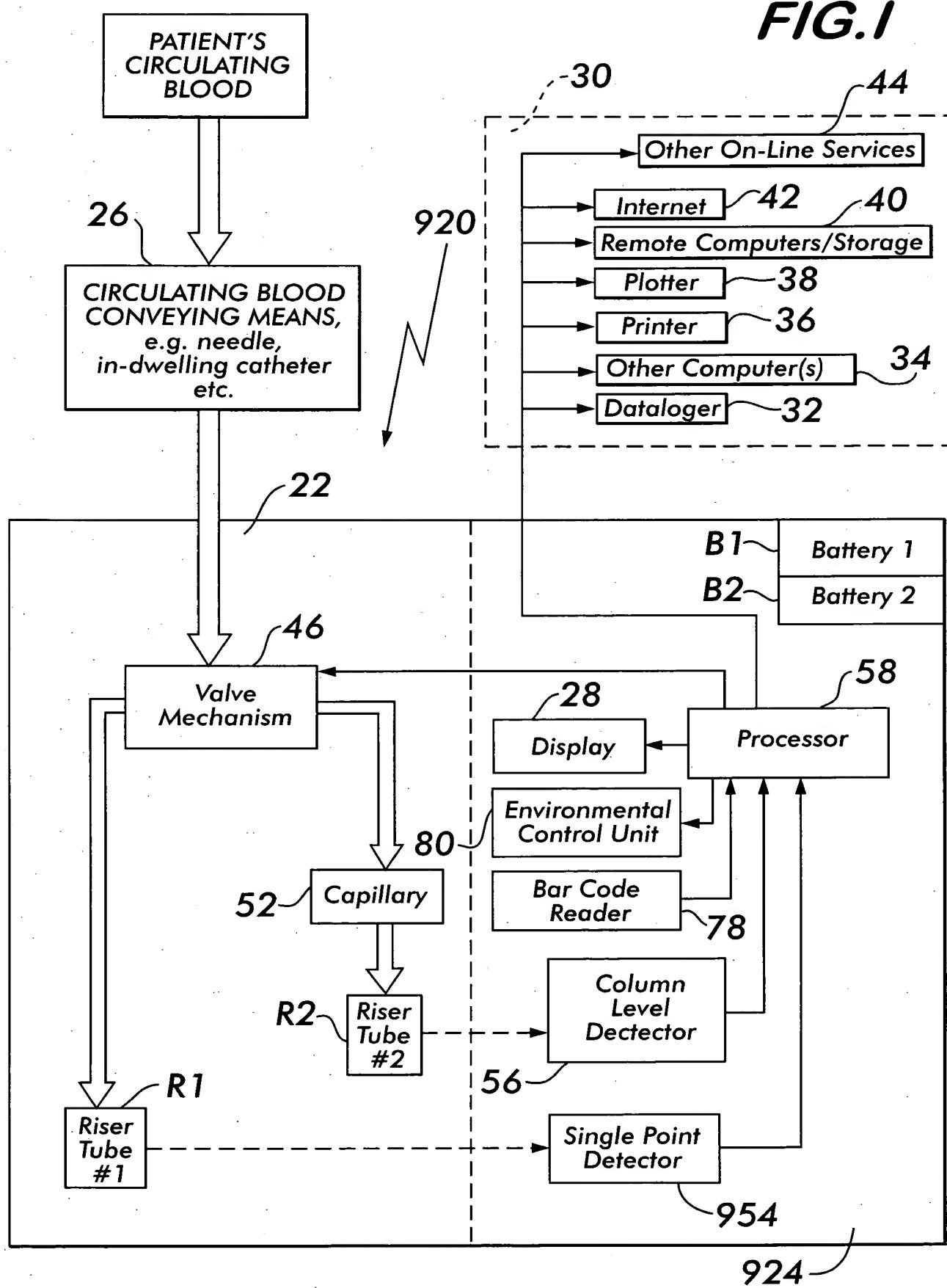


FIG. 2

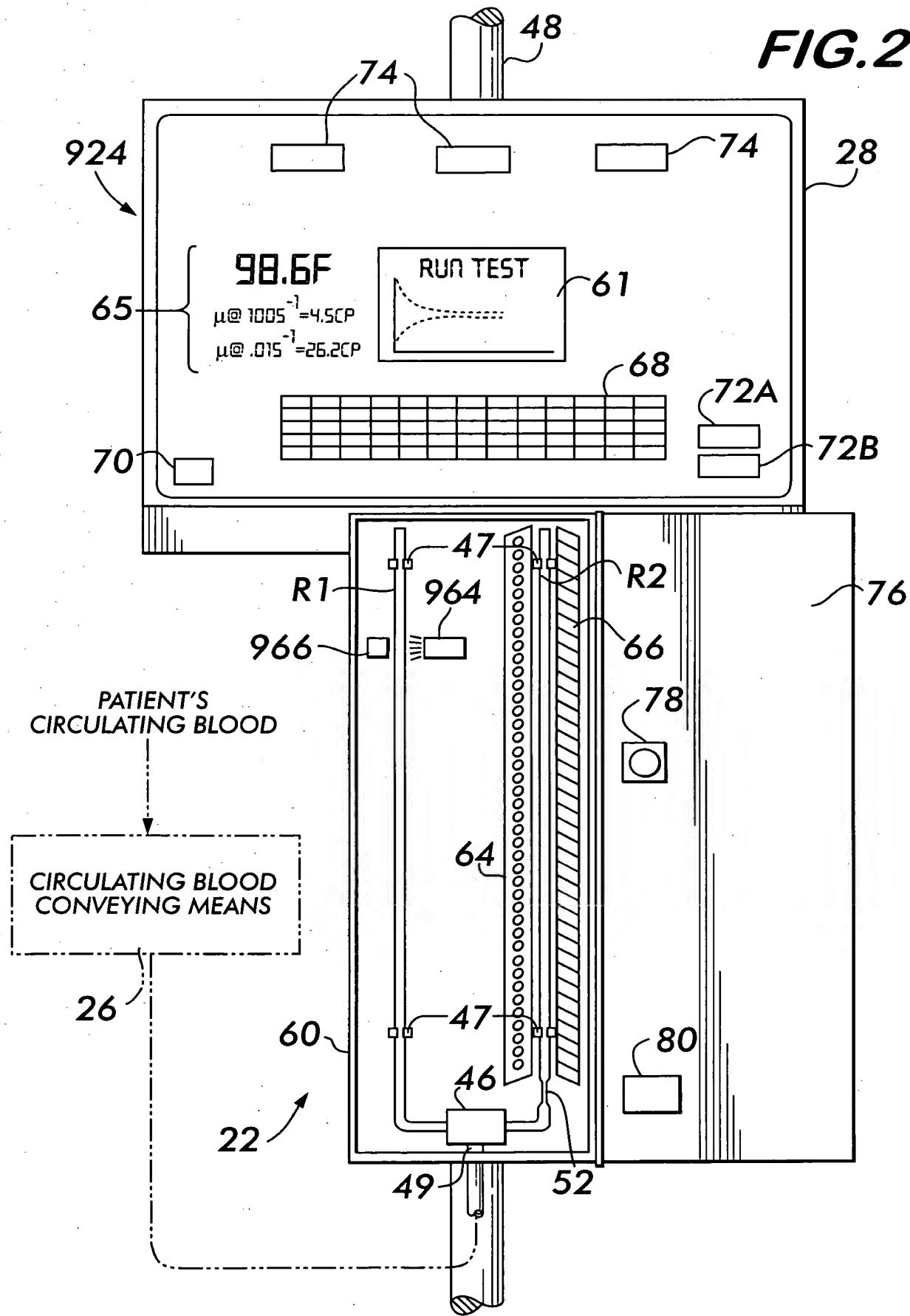


FIG. 3

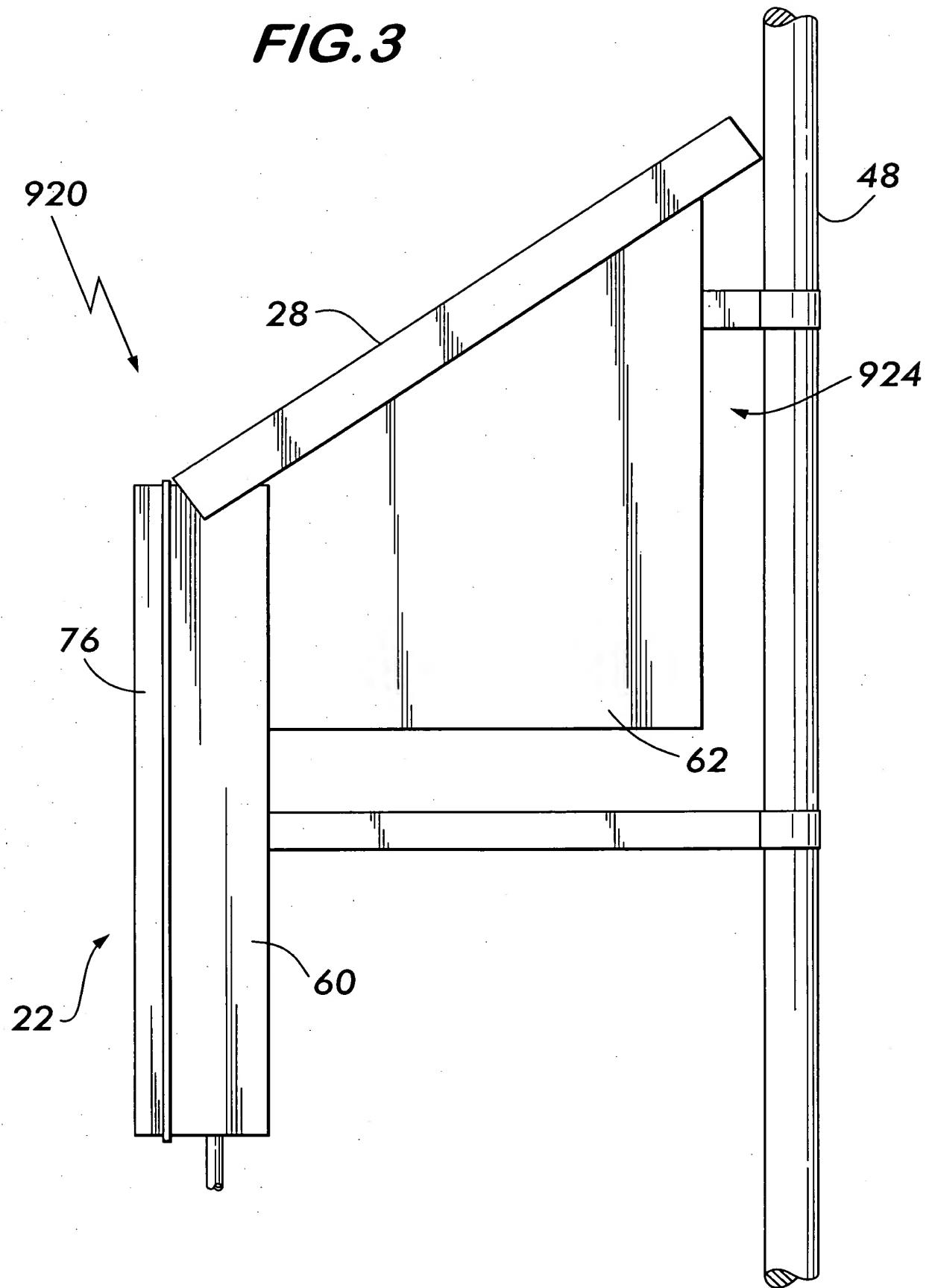


FIG. 4

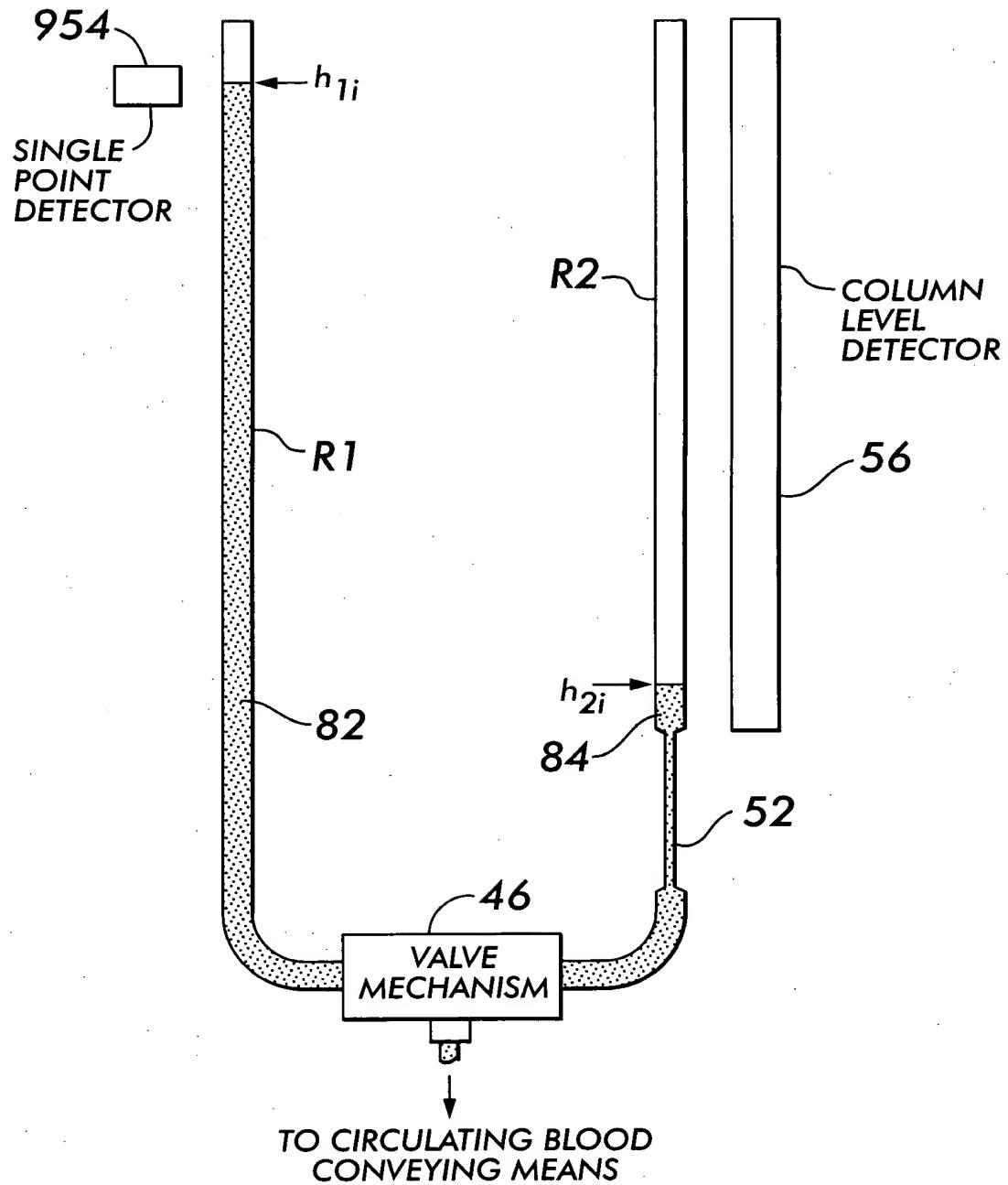


FIG. 5

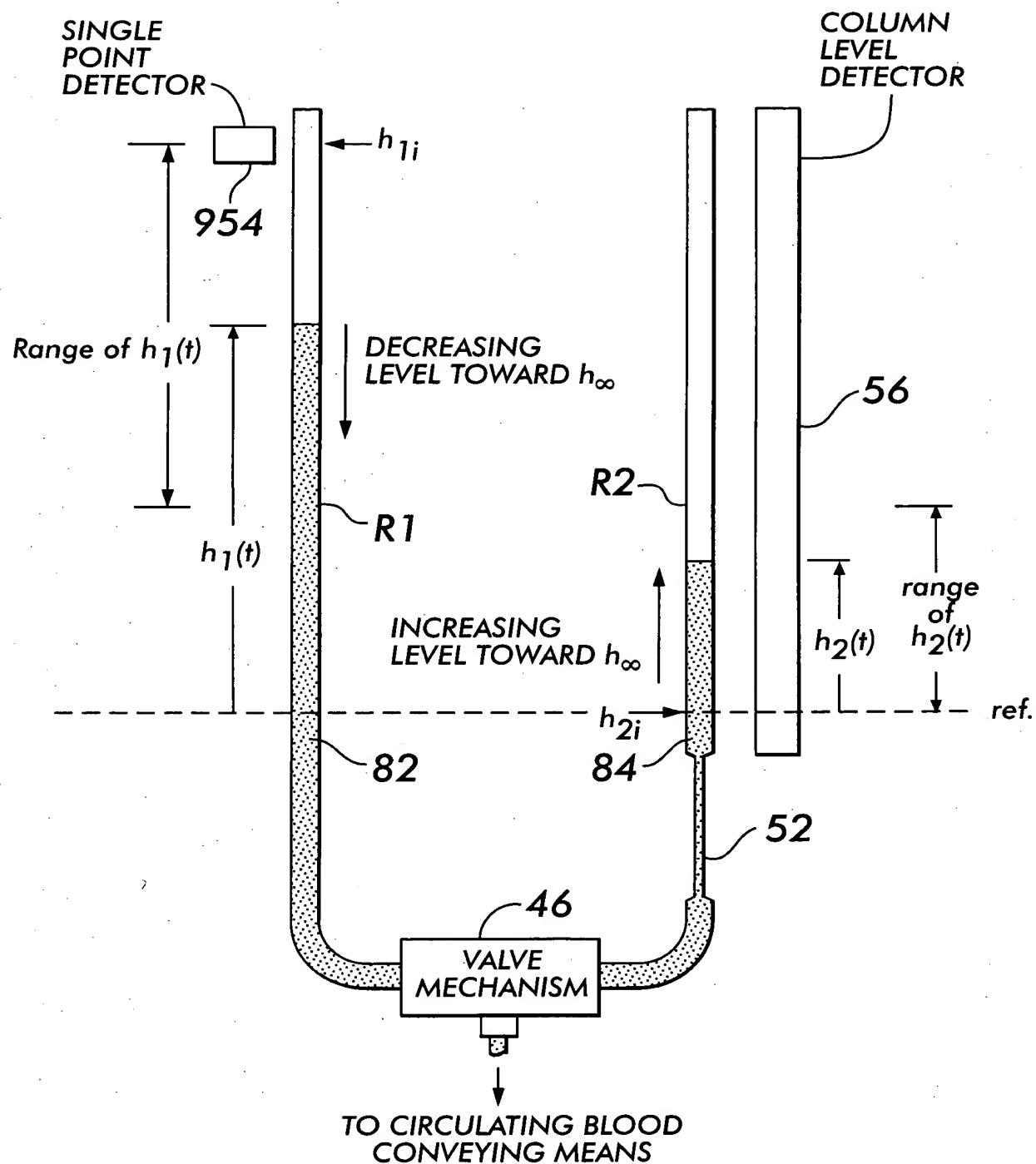
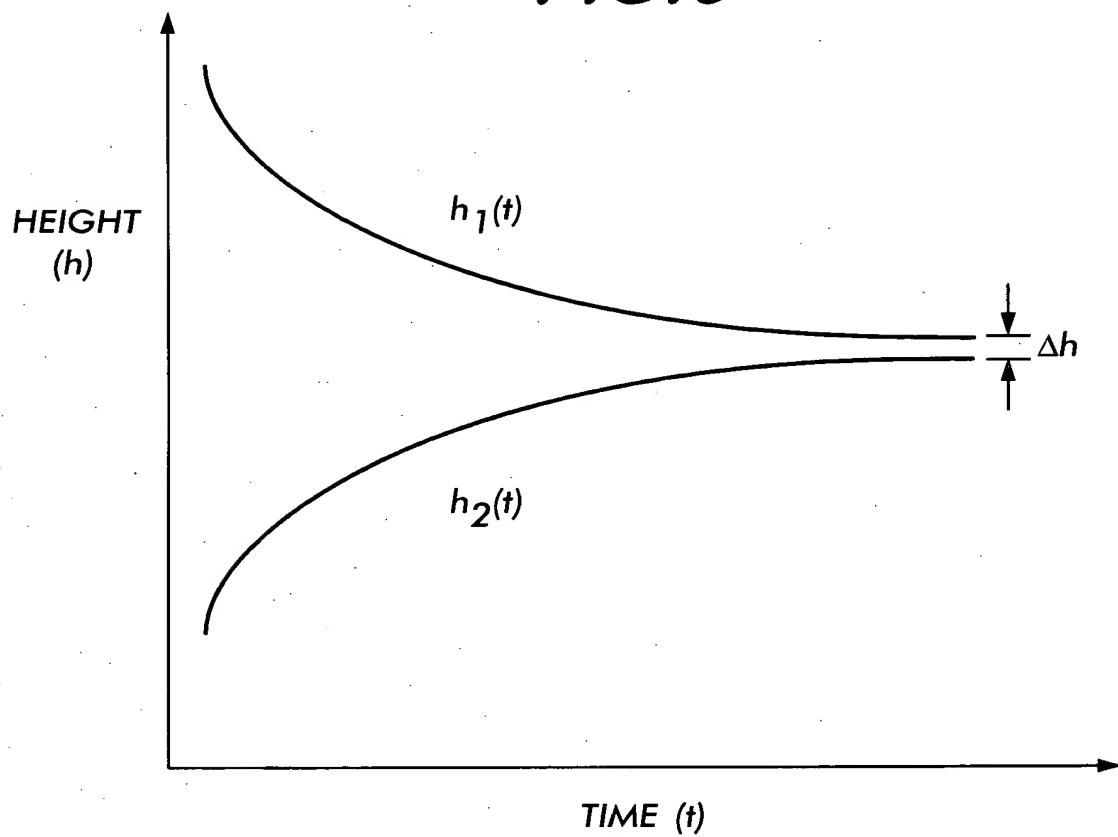


FIG. 6



FROM PROCESSOR 58

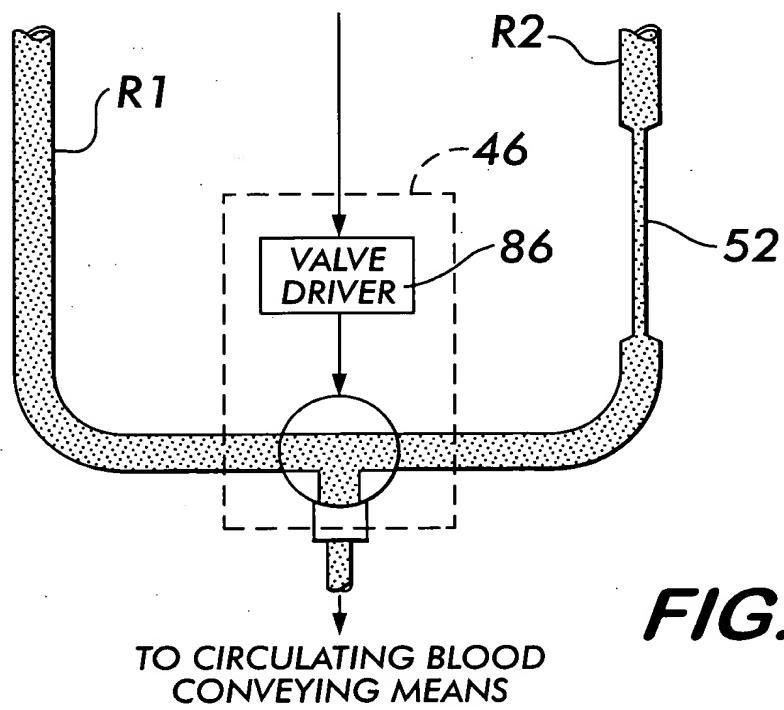


FIG. 7A

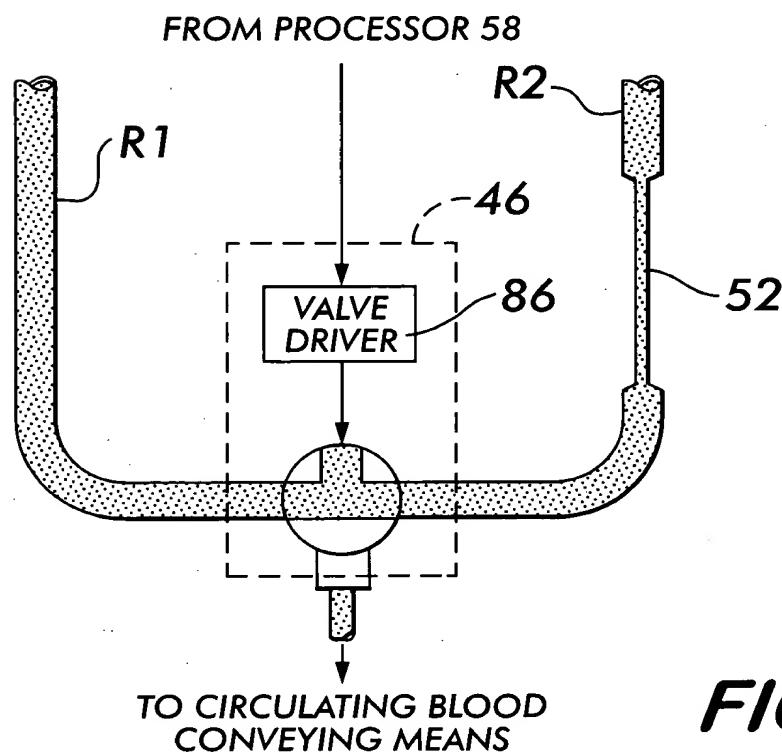
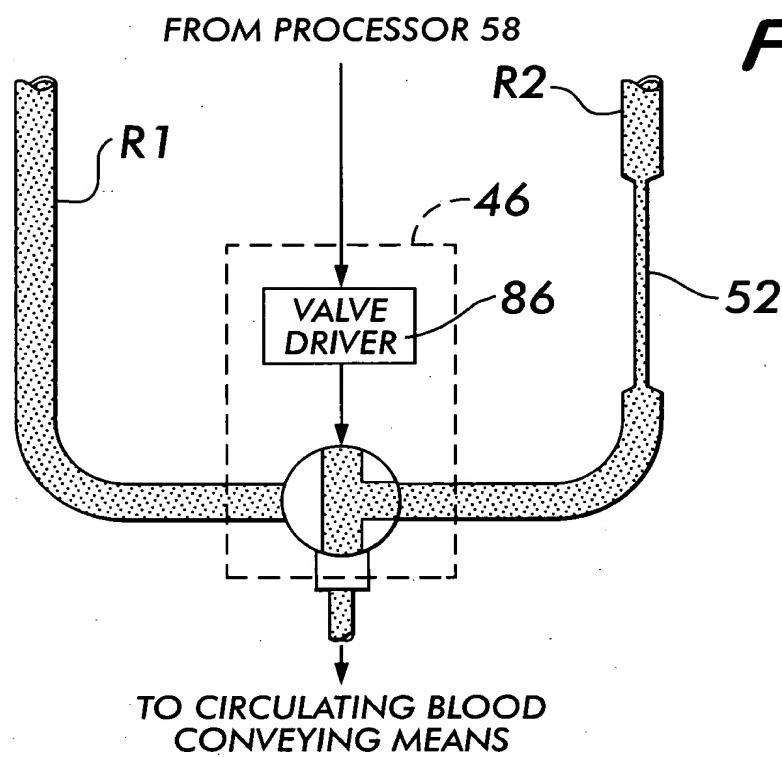
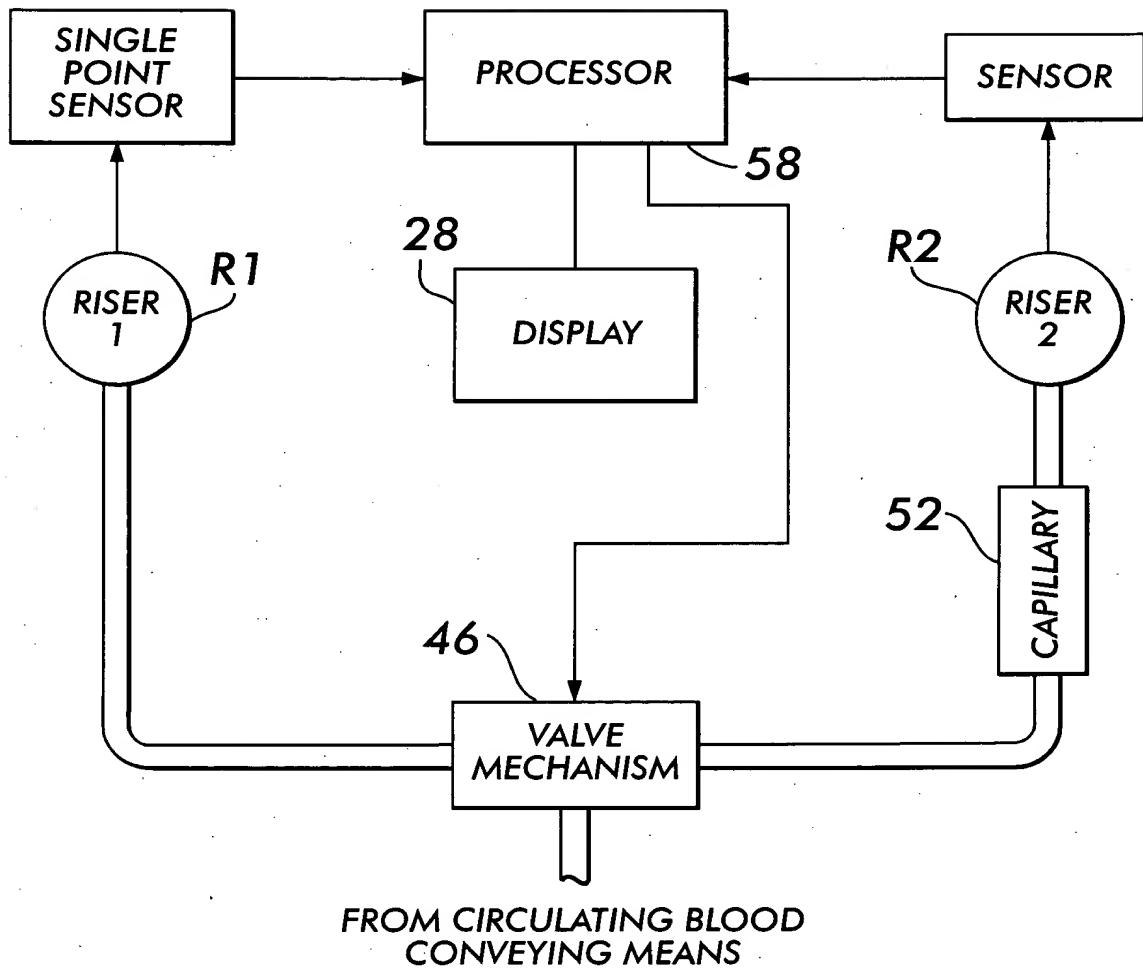
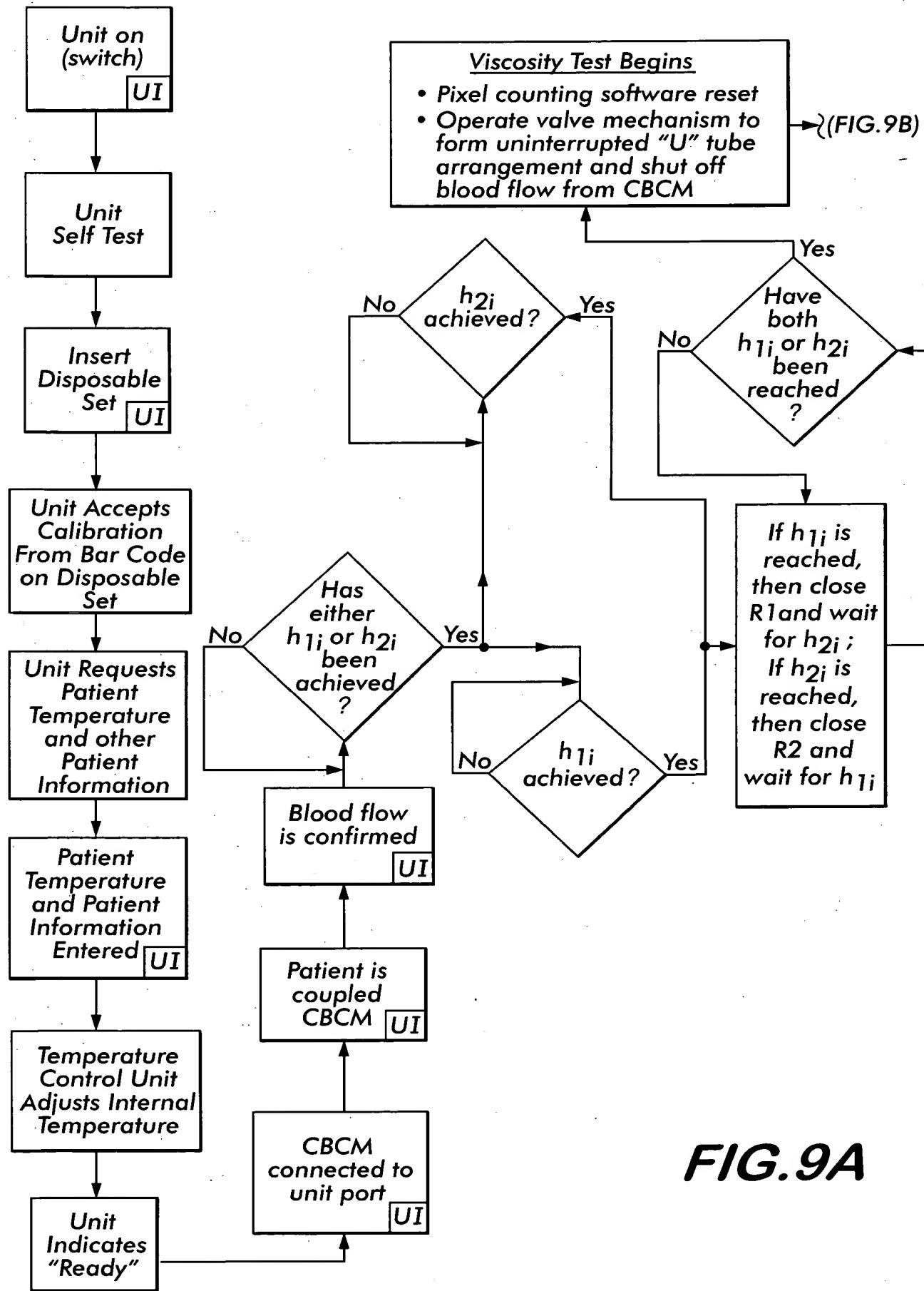


FIG.8

100-000000000000000000000000000000





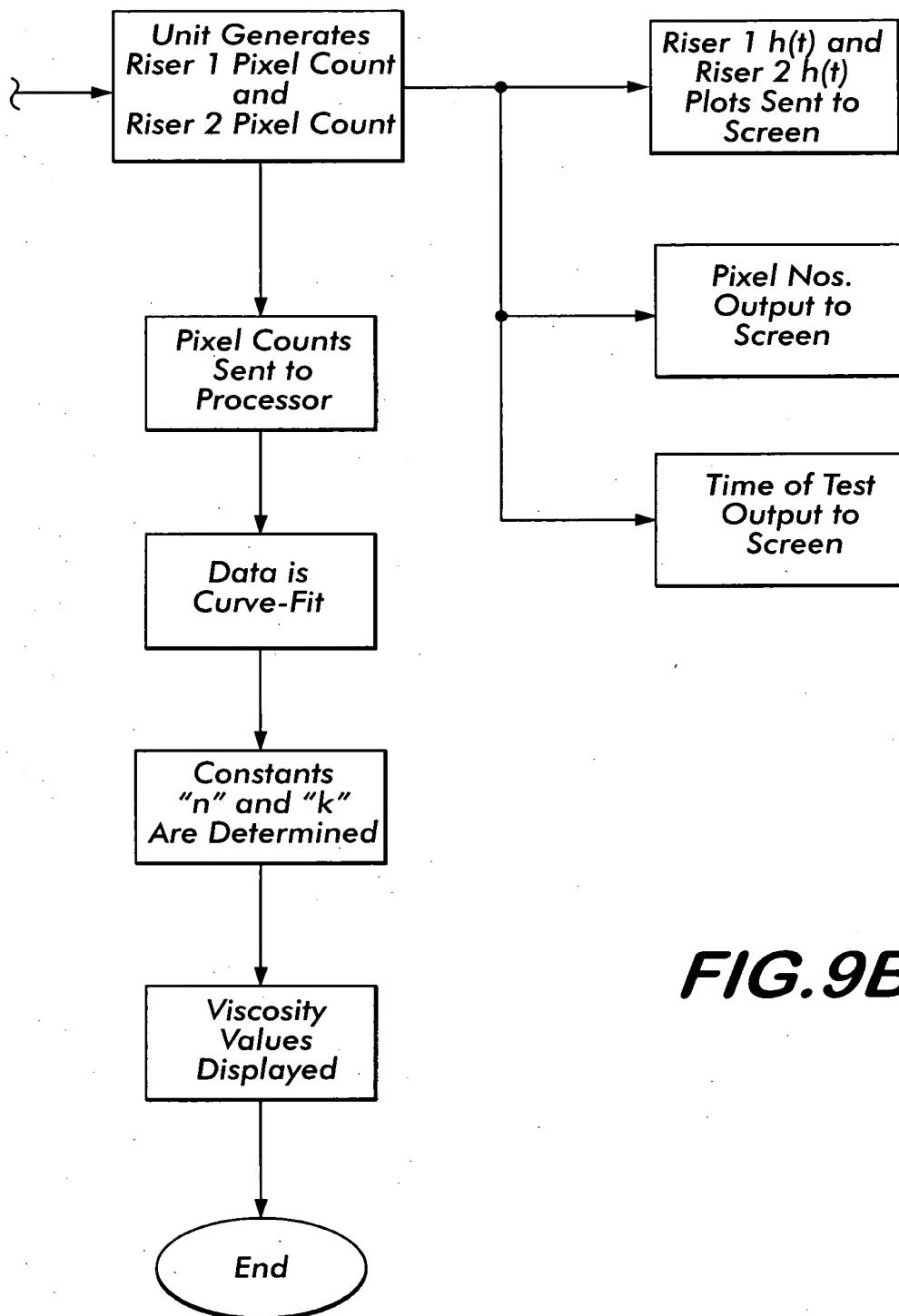


FIG.9B

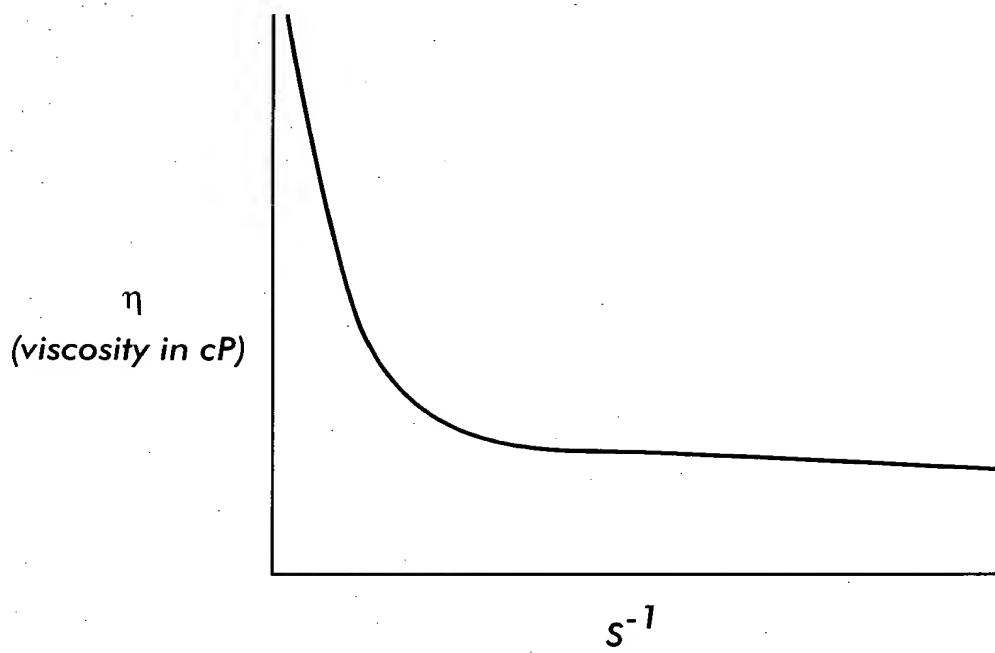


FIG.10A

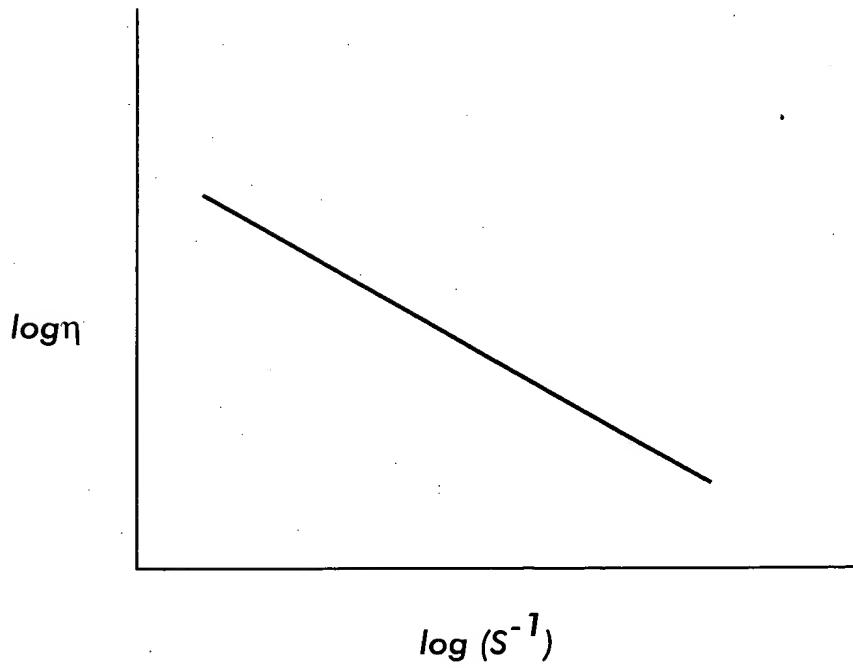


FIG.10B

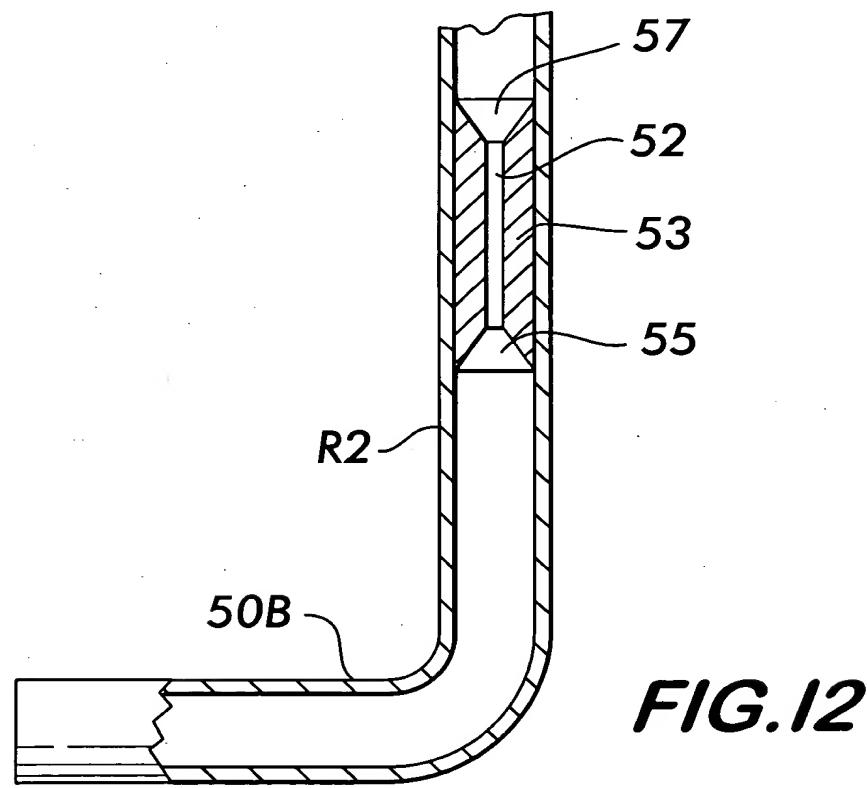
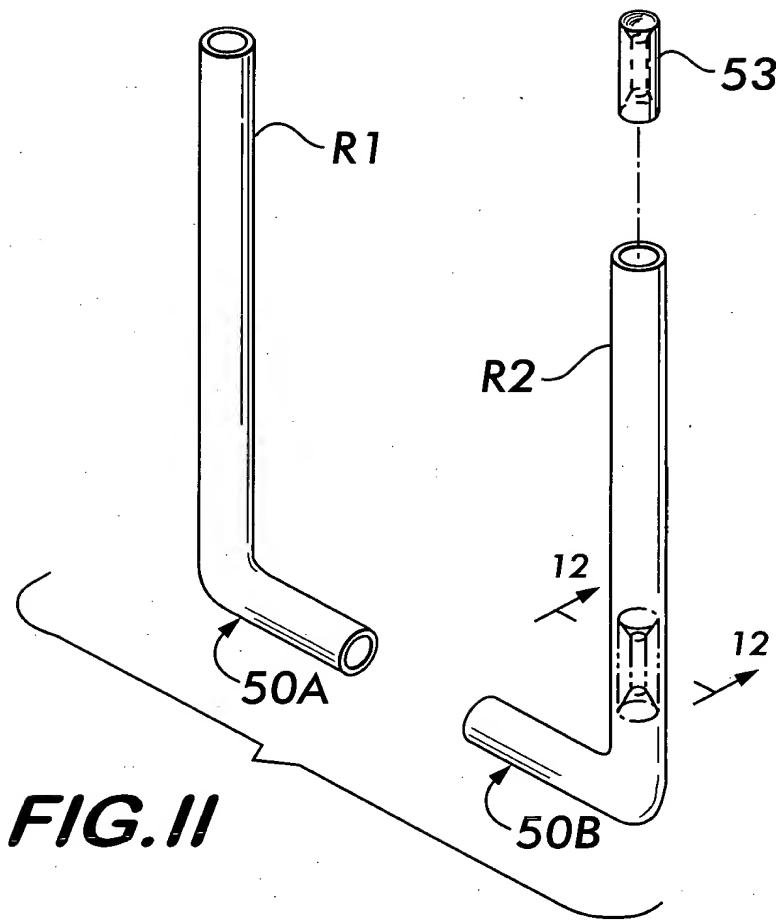


FIG.13

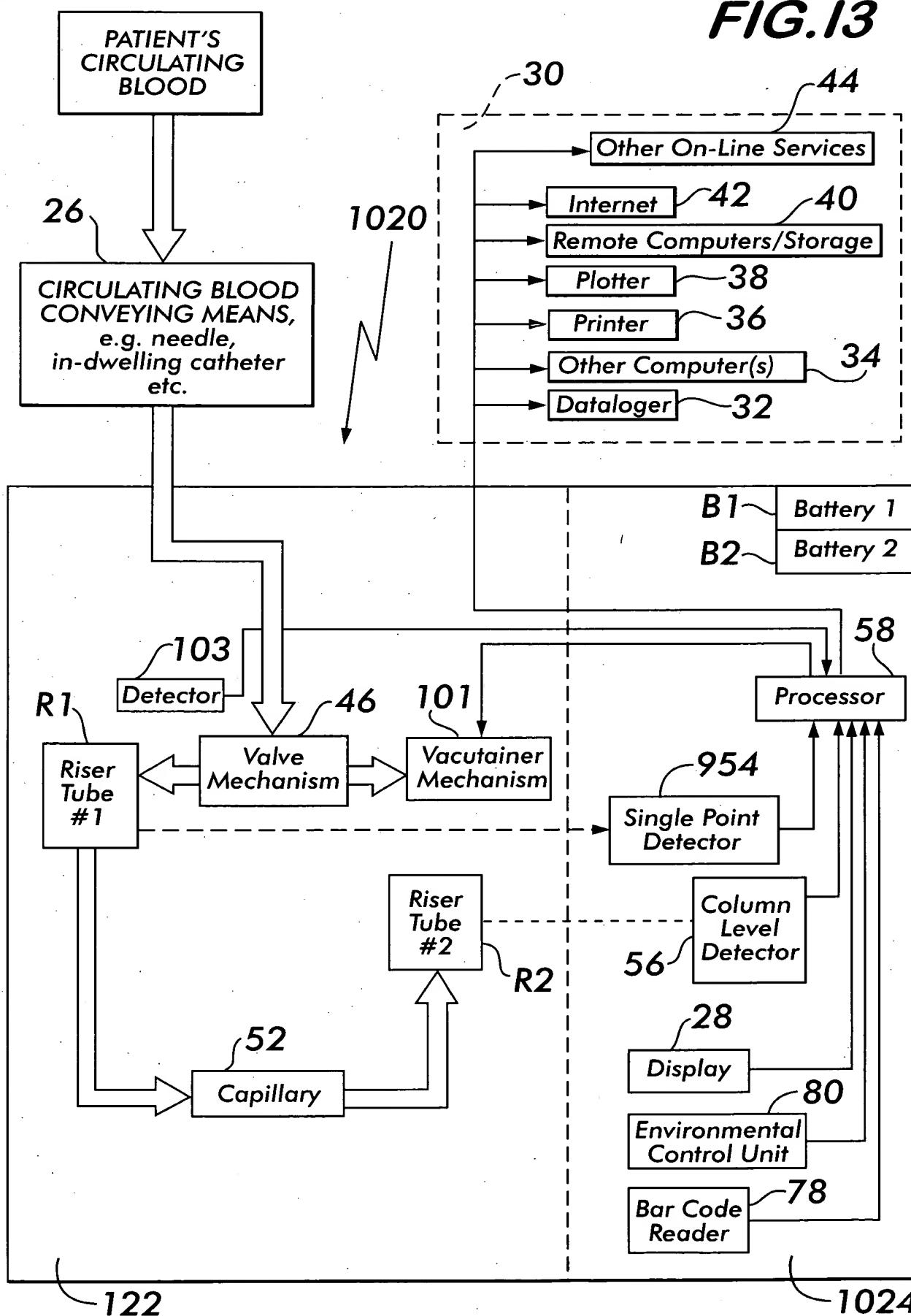


FIG. 14

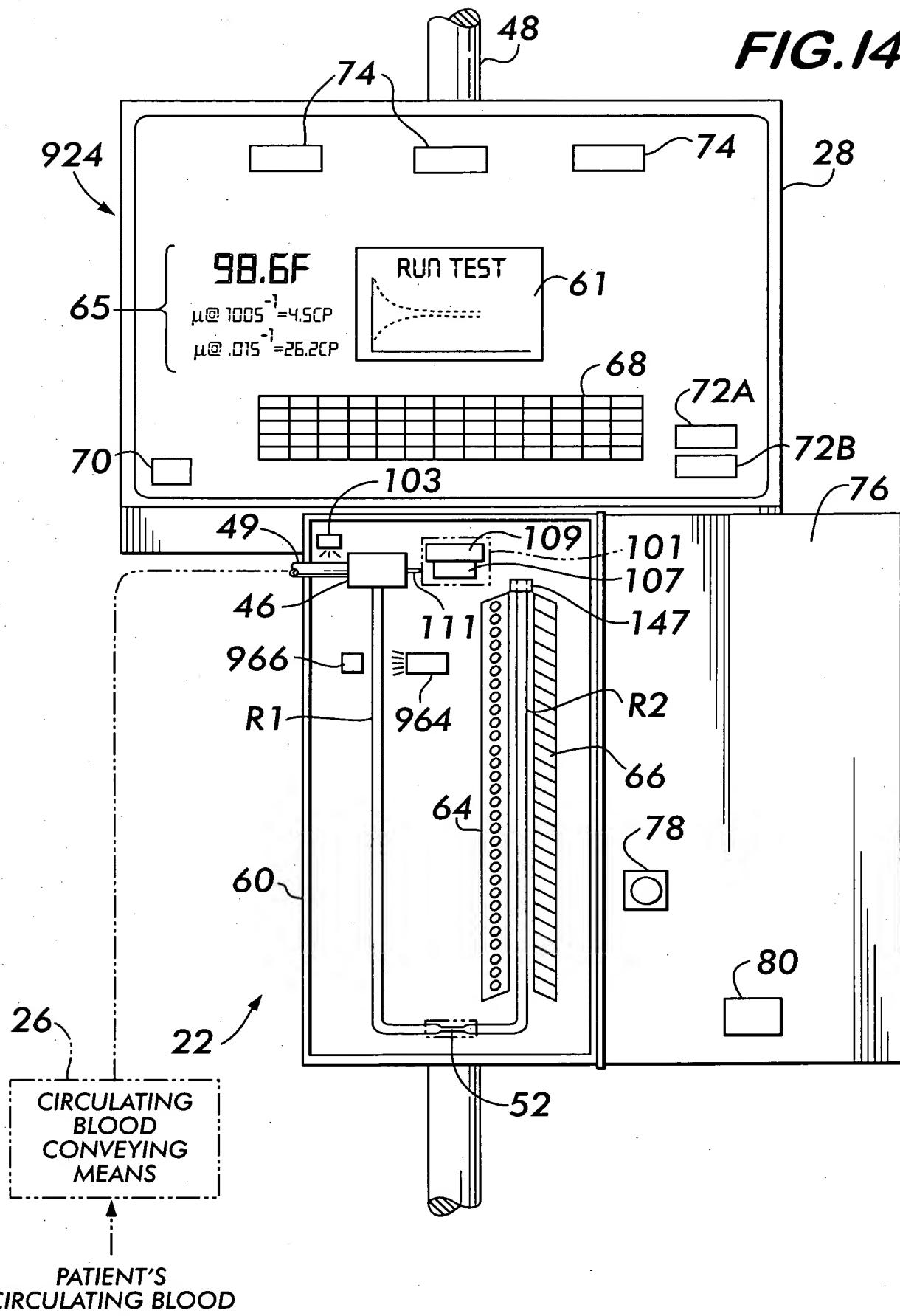


FIG. 15

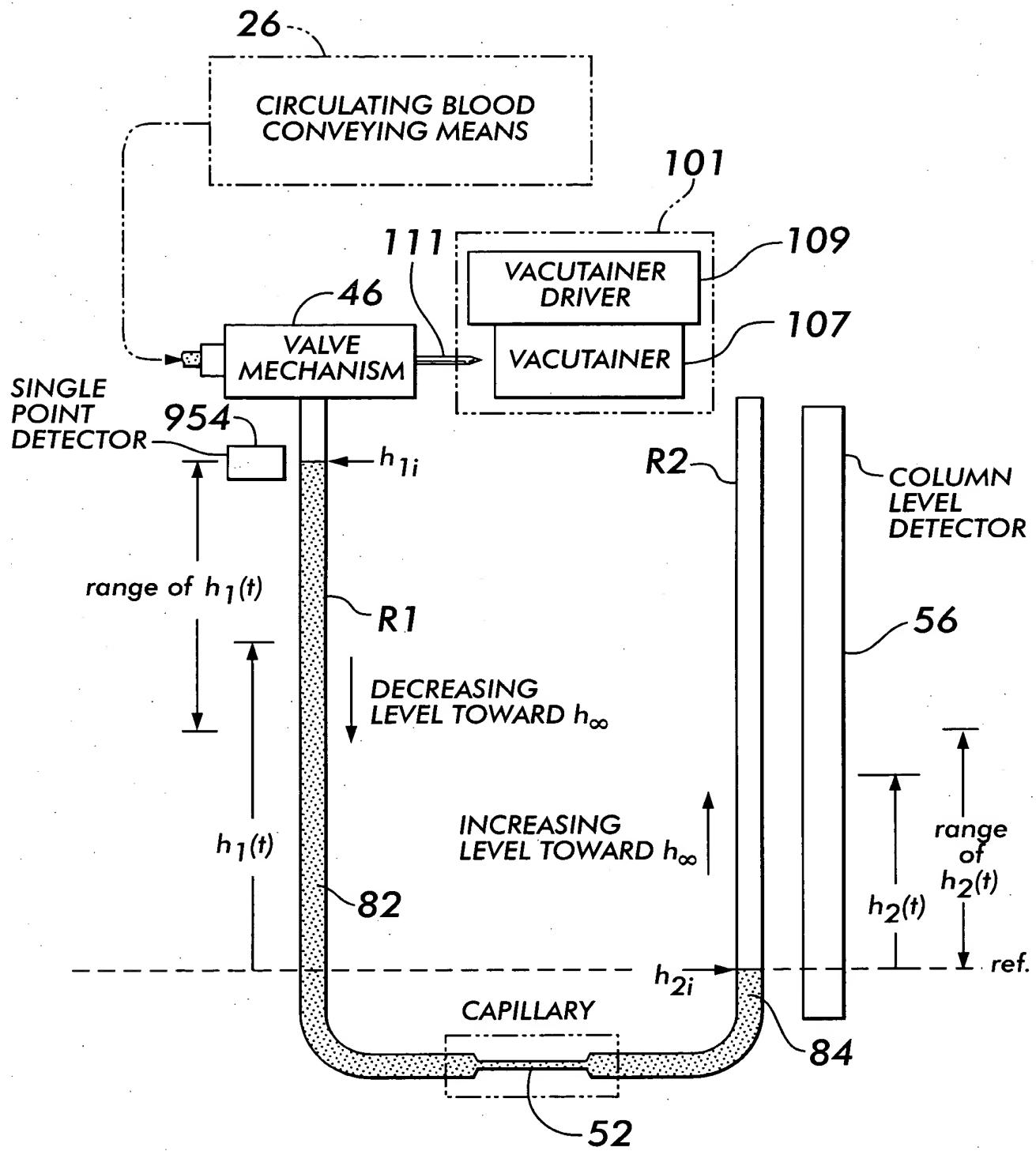
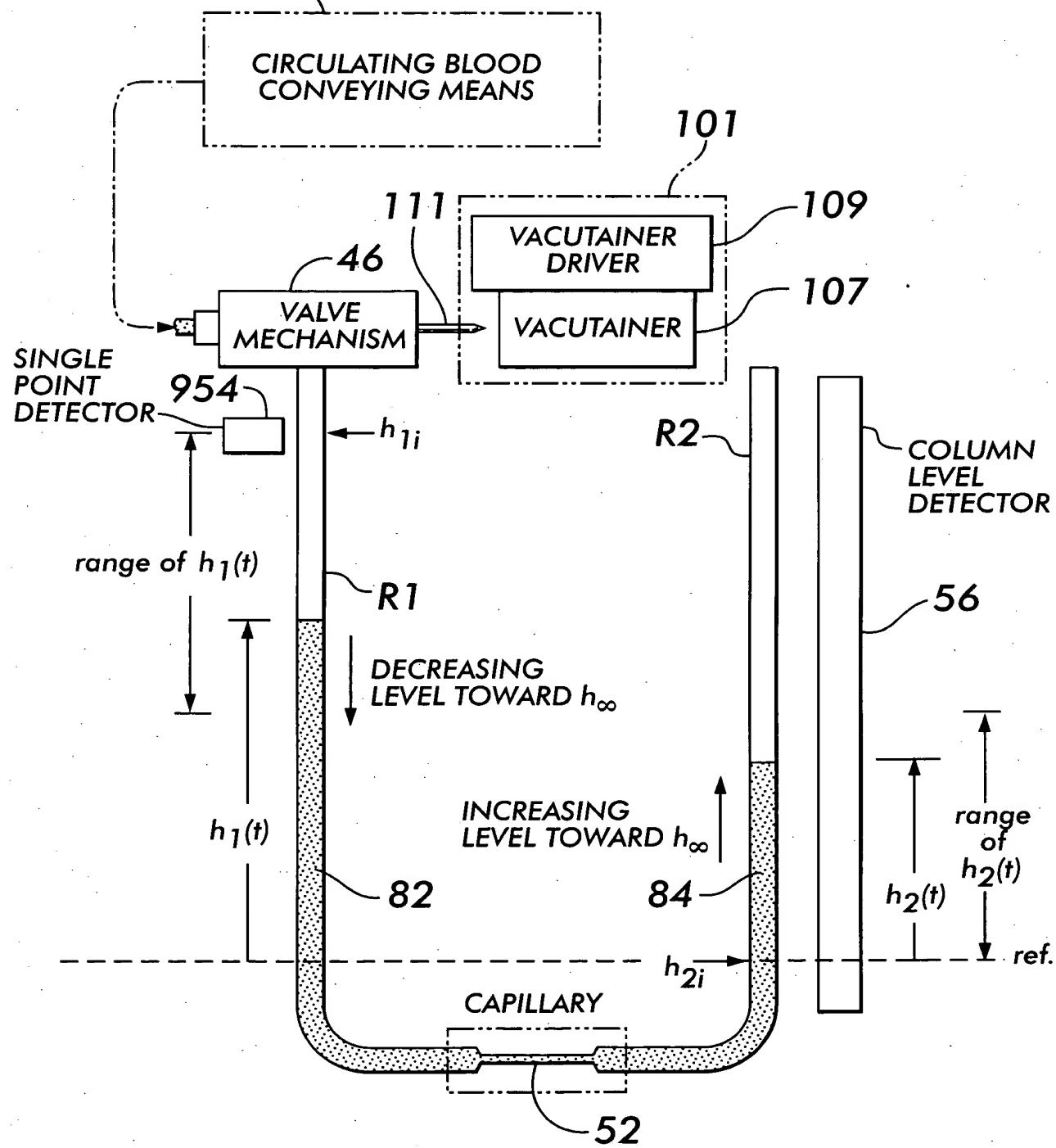


FIG.16

26



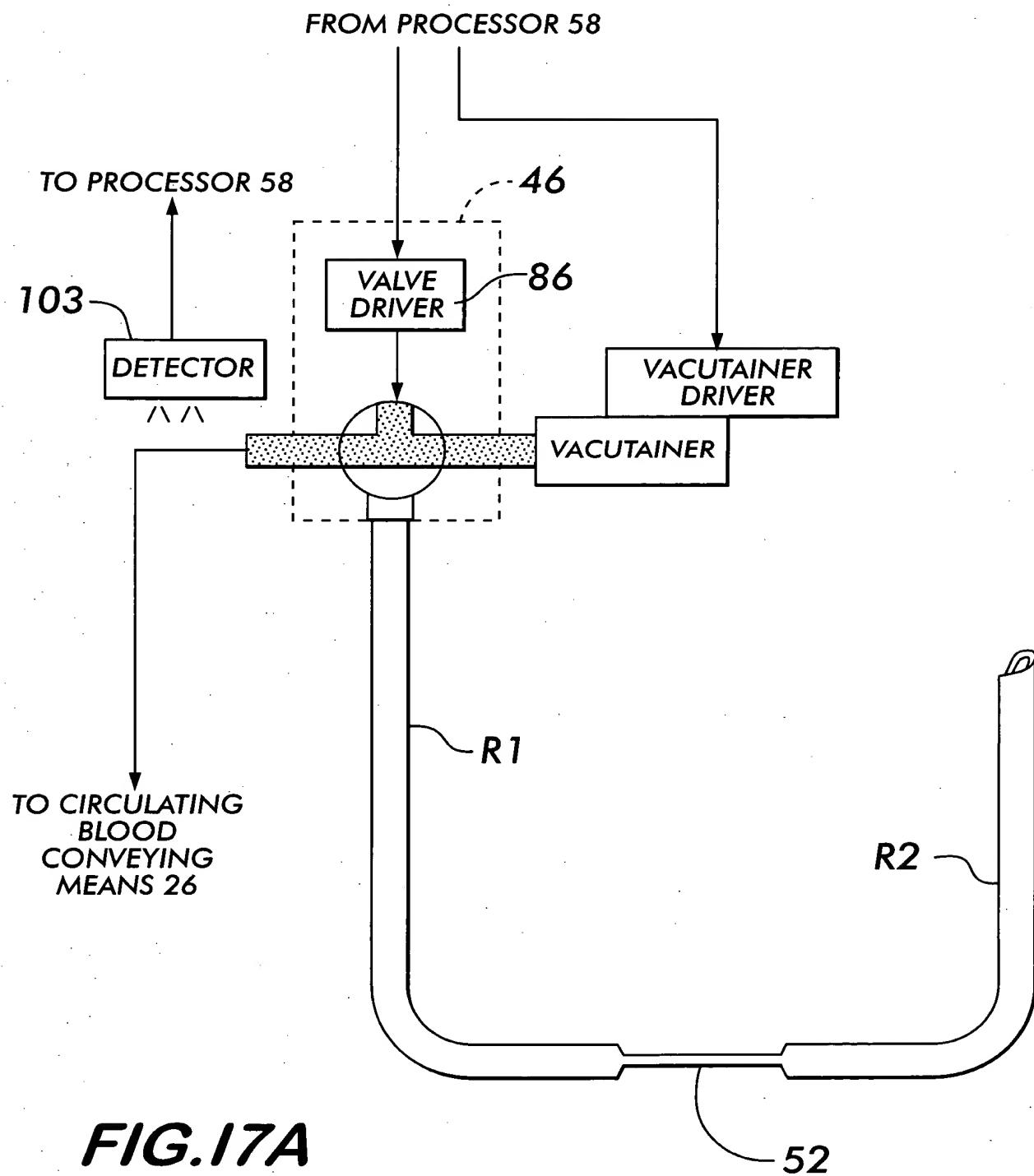


FIG. 17A

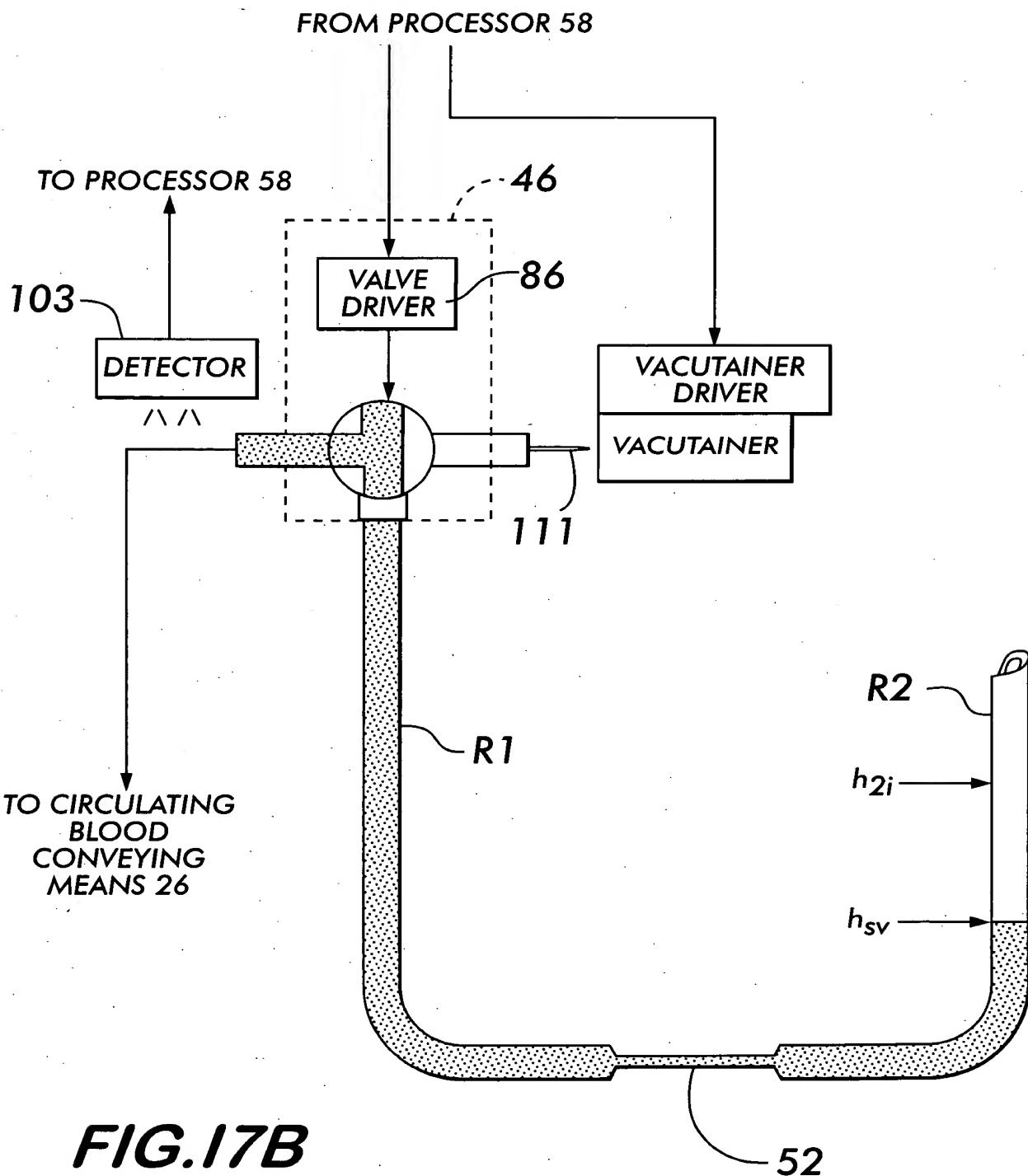


FIG. 17B

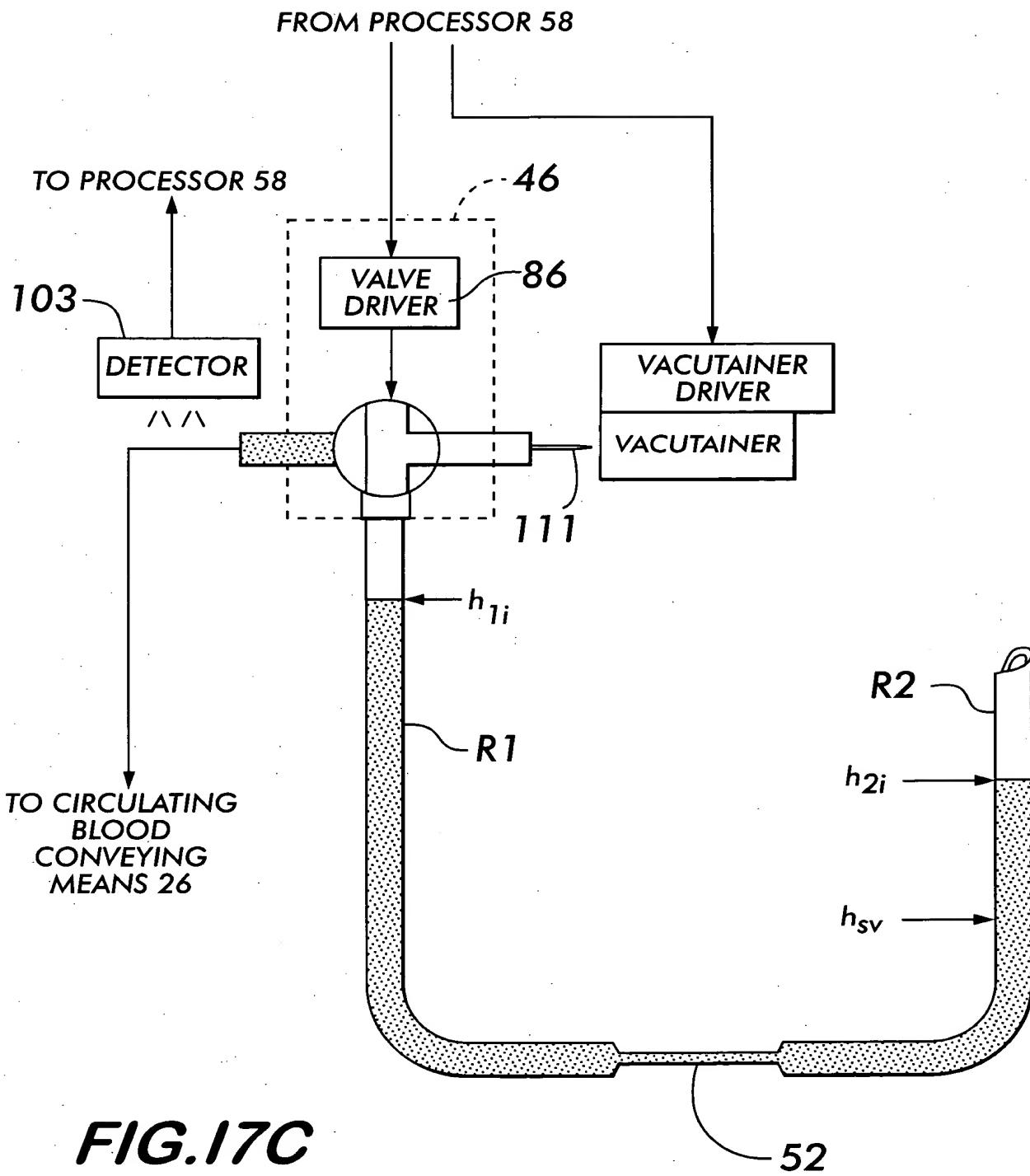


FIG. 18

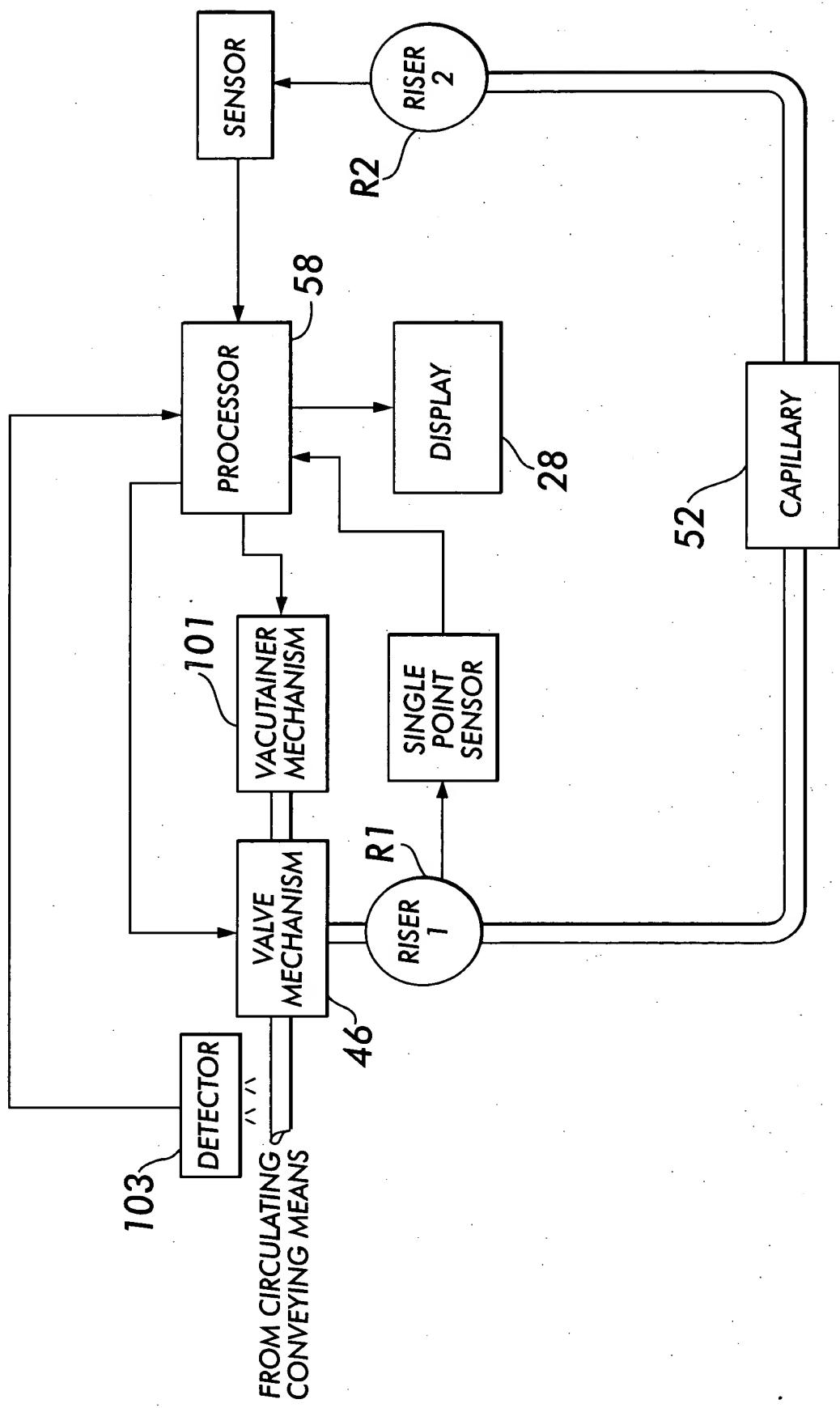
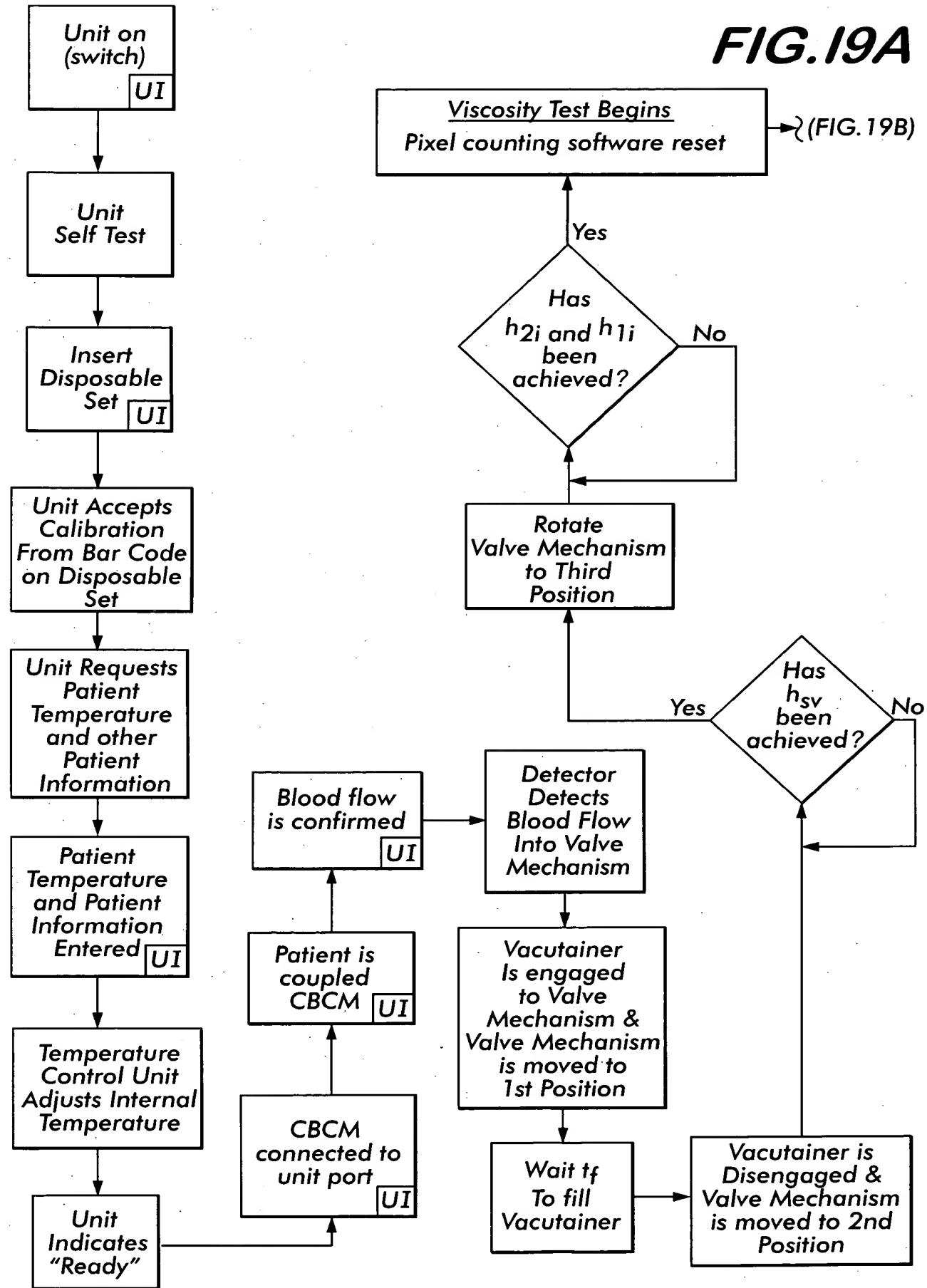


FIG. 19A



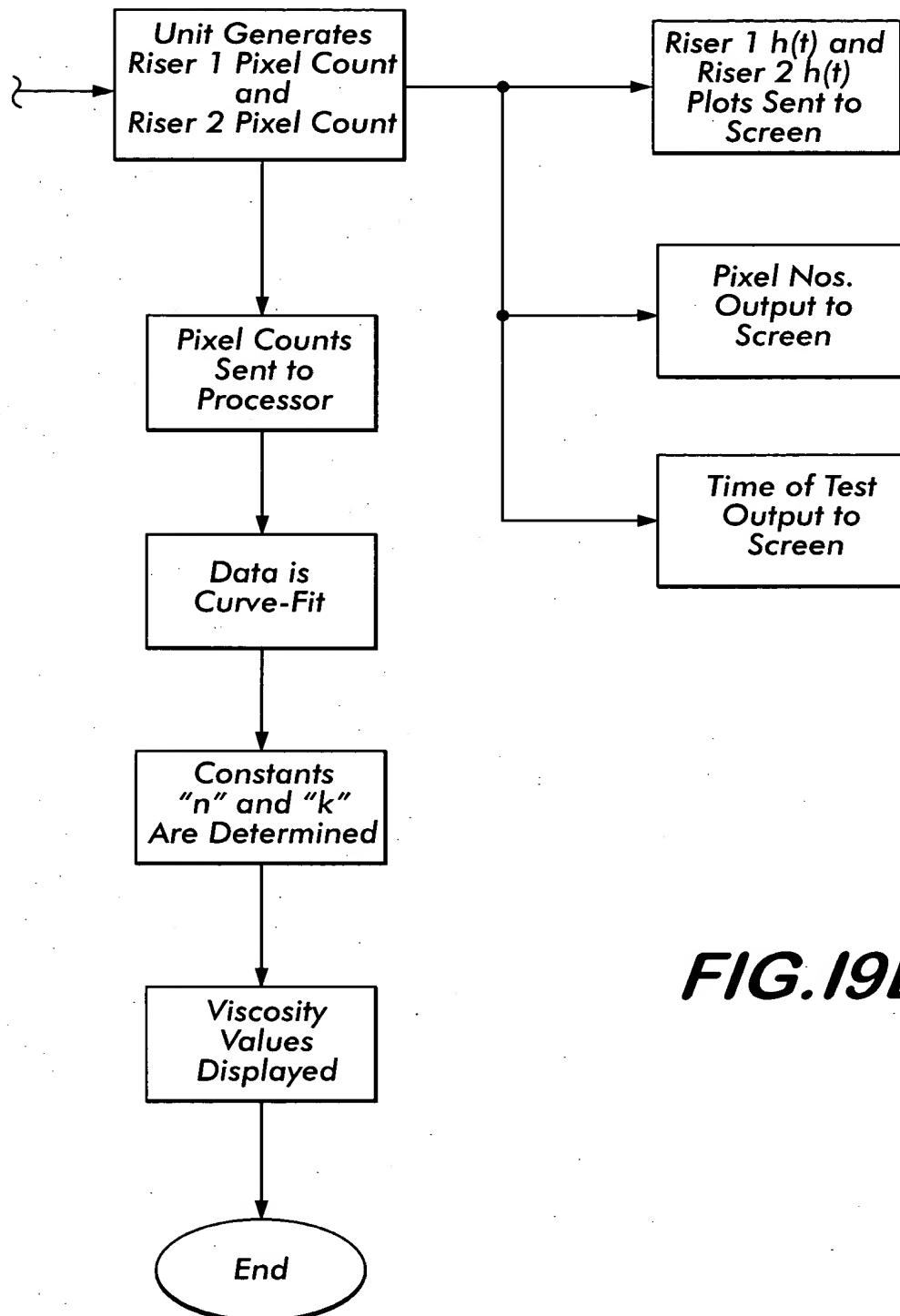


FIG. 19B

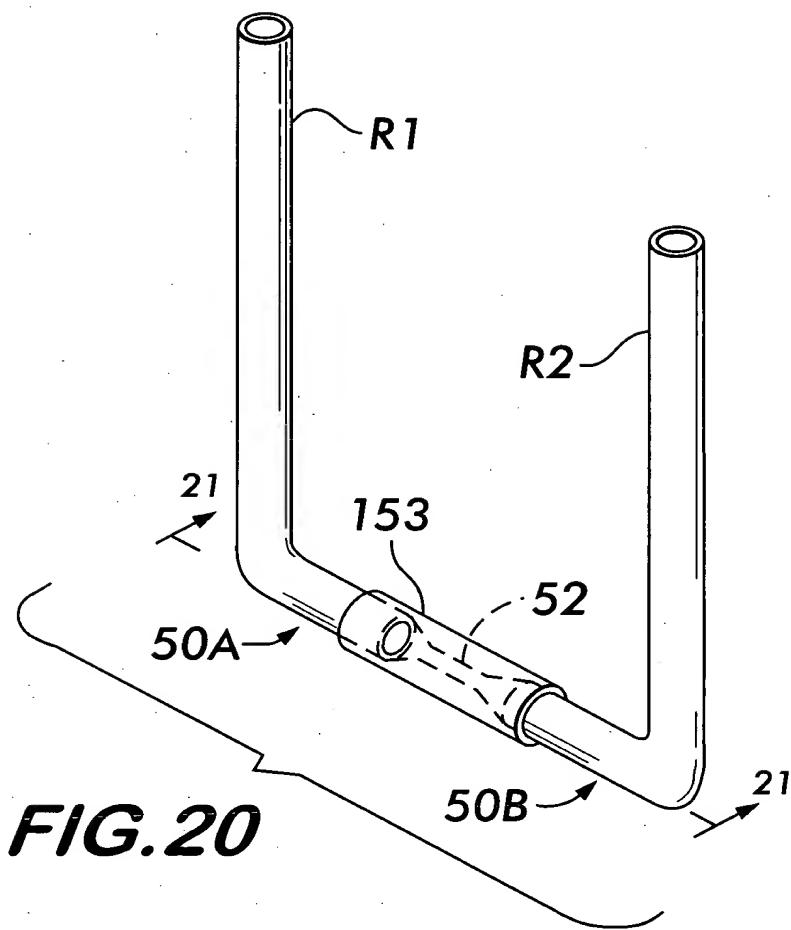


FIG.20

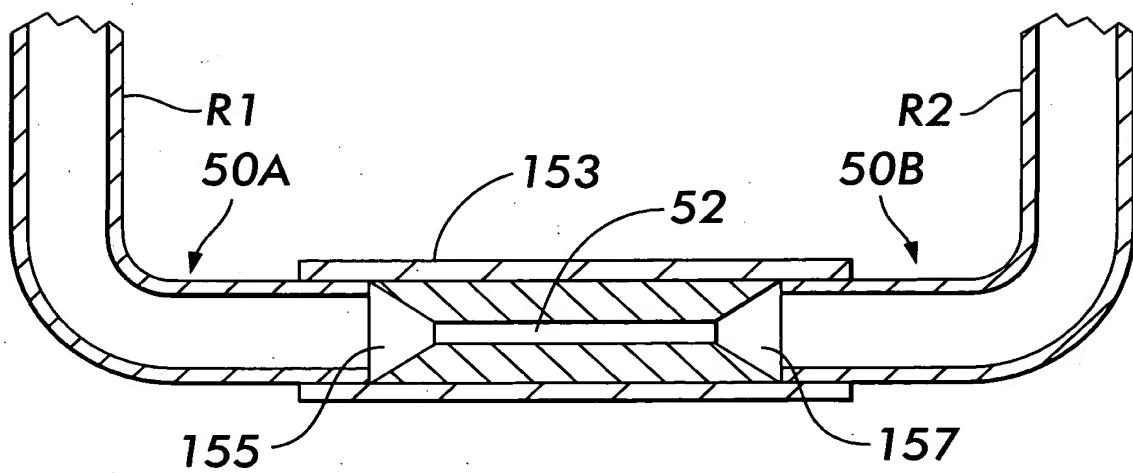


FIG. 21